

Abstracts

Acceleration of Simulated Annealing and its Application to Microwave Device and Circuit Optimization

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Simulated annealing (SA), while being successful as a general optimization technique applicable to many modeling and design problems of microwave devices and circuits, is very time consuming. To alleviate this problem, we propose the creation of a hardware-implemented SA accelerator. The design and evaluation of this SA accelerator, as well as its application to the microwave CAD area, are presented. This accelerator features a highly parallel pipeline structure with a programmable characteristic function. Acceptance prediction is used to further improve the performance. It is evident from simulation results that this accelerator has a significant (several orders of magnitude) speed advantage over an ordinary software implementation.

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